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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,623	11/17/2005	Hjalmar Edzer Ayco Huitema	NL030534US1	1486

24738 7590 04/17/2007

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/557,623	HUITEMA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *November 17, 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

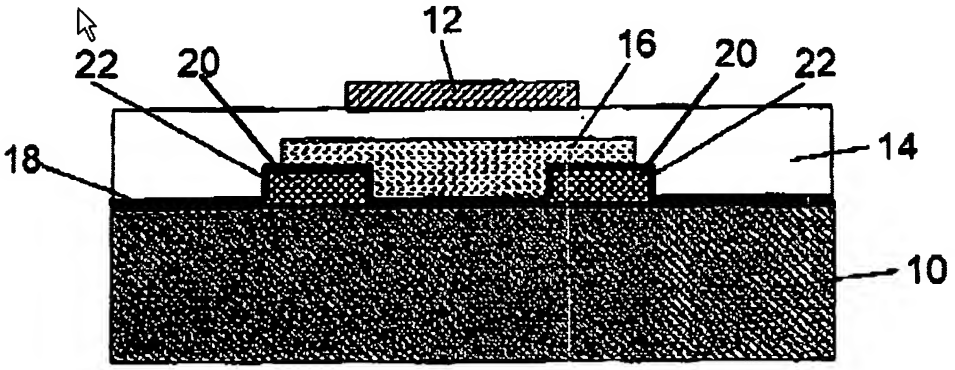
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Dimitrakopoulos et al., U.S. Patent Application Publication No. US 2004/0161873 A1.

Dimitrakopoulos discloses a semiconductor process and device as claimed. Please see **FIGS. 1a-7h**, where Dimitrakopoulos teaches the following limitations.



3. Pertaining to claim 1, Dimitrakopoulos teaches a method of manufacturing an electronic device, in which method at least one field effect transistor is provided on a substrate, which provision of the at least one field effect transistor comprises the steps of:

applying a patterned first conductor layer 20 on the substrate 10;

applying an organic semiconductor layer 16 on the first conductor layer;

applying a dielectric layer 14 on the semiconductor layer;

patterning the organic semiconductor layer and the dielectric layer together; and

applying a patterned second conductor layer 12 on the patterned dielectric layer.

4. Pertaining to claim 2, Dimitrakopoulos teaches a method as claimed as in claim 1 wherein the sep of patterning the organic semiconductor layer and the dielectric layer comprises removing the organic semiconductor layer and the dielectric layer from areas not associated with the at least one field effect transistor and from areas not associated with crossing conductors of the first and second conductor layer (please note that the examiner takes the position that since Dimitrakopoulos teaches a semiconductor substrate such as silicon see paragraph [0048] it is well known to provide field isolation structures so as to separate the different mosfets and the dielectric layer for making just one mosfet on a substrate is inherently patterned).

5. Pertaining to claim 3, Dimitrakopoulos teaches a method as claimed in claim 2, wherein the said areas associated with a field effect transistor and/or the said areas associated with crossing conductors include protection zones providing a minimal lateral distance between a first conductor in the first conductor layer and second conductor layer in the second conductor layer (the Examiner takes the position that the protection zone is layer 18).

6. Pertaining to claim 4, Dimitrakopoulos teaches a method as claimed in claim 1 wherein the step of applying an organic semiconductor layer on the first conductor layer comprises applying an organic semiconductor or a precursor thereof by spin coating (see paragraph [0054]).

7. Pertaining to claim 5, Dimitrakopoulos teaches a method as claimed in claim 1 wherein the dielectric layer comprises an initiator sensitive for actinic radiation and functions after irradiation as a mask for the patterning of the semiconductor layer (see paragraph [0058]).

8. Pertaining to claim 6, Dimitrakopoulos teaches a method as claimed in claim 4, wherein the dielectric comprises a photoresist material.

9. Pertaining to claim 7, Dimitrakopoulos teaches a method as claimed in claim 1, comprising the additional step of providing an electro-optical layer so as to provide a display arrangement (because Dimitrakopoulos teaches a active matrix liquid crystal display it is well known to passivate the pixels with a transparent material, see paragraph [[0002]).

10. Pertaining to claim 8, Dimitrakopoulos teaches a method as claimed in claim 6 wherein the substrate is substantially transparent (please note that Dimitrakopoulos teaches various substrates such as SiO_2 and sapphire which are inherently transparent).

11. Pertaining to claim 9, Dimitrakopoulos teaches an electronic device comprising a plurality of field effect transistor on a substrate and an interconnect structure so as to connect the

transistors mutually and/or to an output terminal, the field effect transistor and at least part of the interconnect structure being provided in a stack of:

a patterned first conductor layer applied on the substrate;

an organic semiconductor layer applied on the first conductor layer;

a dielectric layer applied on the semiconductor layer;

wherein the semiconductor layer and the dielectric layer are provided in substantially identical pattern (please note that since the dielectric layer covers the semiconductor layer substantially by a conformal deposition process, the claimed limitation has been met).

12. Pertaining to claim 10, Dimitrakopoulos teaches an electronic device as claimed in claim 9, wherein the semiconductor layer and the dielectric layer are absent from areas not associated with the field effect transistor and from areas not associated with crossing conductors of the first and second conductor layer (please note that the Examiner takes note that the claimed materials are missing on the underside of substrate 10).

Double Patenting

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 1-10 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of copending Application No. 10/547,591. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well known to apply a photoresist for patterning films for semiconductor devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Specification

15. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

16. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

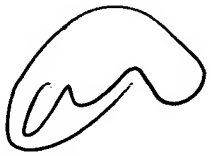
17. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "307" has been used to designate both semiconductor layer and dielectric layer. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC